



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

11.2

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/811,207	03/26/2004	Cheisan J. Yue	P04,0097 (H0005049,SBE 16	1964
128 7590 08/01/2007 HONEYWELL INTERNATIONAL INC. 101 COLUMBIA ROAD P O BOX 2245 MORRISTOWN, NJ 07962-2245			EXAMINER LEWIS, MONICA	
			ART UNIT 2822	PAPER NUMBER
			MAIL DATE 08/01/2007	DELIVERY MODE PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	<b>Application No.</b> 10/811,207	<b>Applicant(s)</b> YUE ET AL.	
	<b>Examiner</b> Monica Lewis	<b>Art Unit</b> 2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 11 May 2007.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1-39 is/are pending in the application.
- 4a) Of the above claim(s) 20-39 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-19 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 26 March 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)                                | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                       | 5) <input type="checkbox"/> Notice of Informal Patent Application                       |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

### **DETAILED ACTION**

1. This office action is in response to the request for continued examination filed May 11, 2007.

#### ***Continued Examination Under 37 CFR 1.114***

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 5/11/07 has been entered.

#### ***Response to Arguments***

3. Applicant's arguments with respect to claims 1-19 have been considered but are moot in view of the new ground(s) of rejection.

#### ***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Art Unit: 2822

5. Claims 1, 2, 5, 6, 9, 10, 13, 14 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Librizzi et al. (U.S. Patent No. 6,429,502) in view of Clevenger et al. (U.S. Patent No. 6,573,565).

In regards to claim 1, Librizzi et al. ("Librizzi") discloses the following:

- a) a semiconductor substrate (40) (For Example: See Figure 2);
- b) a buried insulation layer (42) over the semiconductor substrate (For Example: See Figure 2);
- c) a semiconductor mesa (28 or 34) over the buried insulation layer (For Example: See Figure 1 and Figure 2); and
- d) a guard ring (36 and 38) substantially surrounding the semiconductor mesa, and wherein the guard ring is arranged to provide RF isolation for the semiconductor mesa (For Example: See Figure 1 and Column 5 Lines 55-57).

In regards to claim 1, Librizzi fails to disclose the following:

- a) the guard ring extends through the buried insulation layer contacting the semiconductor substrate.

However, Clevenger et al. ("Clevenger") discloses a semiconductor device that has a guard ring (210) that extends through the buried insulation layer (203) contacting the semiconductor substrate (201) (For Example: See Figure 2). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Librizzi to include a guard ring that extends through the buried insulation layer contacting the semiconductor substrate as disclosed in Clevenger because it aids in providing a conduction path (For Example: See Column 3 Lines 49-67 and Column 4 Lines 1-8).

Additionally, since Librizzi and Clevenger are both from the same field of endeavor, the purpose disclosed by Clevenger would have been recognized in the pertinent art of Librizzi.

Art Unit: 2822

In regards to claims 2, 6, 10 and 14, Librizzi discloses the following:

a) the semiconductor substrate comprises a high resistivity semiconductor substrate (For Example: See Column 5 Lines 19-22).

In regards to claims 5 and 13, Librizzi discloses the following:

a) the semiconductor substrate is doped in an area that is contacted by the guard ring (For Example: See Column 5 Lines 15 and 16).

In regards to claim 9, Librizzi discloses the following:

a) an insulating ring (26) between the guard ring and the semiconductor mesa, wherein the insulating ring surrounds the semiconductor mesa (For Example: See Figure 1).

In regards to claim 17, Librizzi discloses the following:

a) the guard ring comprises a low resistivity guard ring (For Example: See Column 6 Line 6).

6. Claims 3, 4, 7, 8, 11, 12, 15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Librizzi et al. (U.S. Patent No. 6,429,502) in view of Clevenger et al. (U.S. Patent No. 6,573,565) and Beyer et al. (U.S. Patent No. 5,264,387).

In regards to claims 3, 7, 11 and 15, Librizzi discloses the following:

a) the semiconductor substrate comprises a silicon substrate, wherein the buried insulating layer comprises a buried silicon oxide layer (For Example: See Column 5 Lines 14-18).

In regards to claims 3, 7, 11 and 15, Librizzi fails to disclose the following:

a) the semiconductor mesa comprises a silicon mesa.

However, Beyer et al. ("Beyer") discloses a semiconductor device that has semiconductor mesa that comprises a silicon mesa (For Example: See Column 3 Lines 15 and 16). It would have been obvious to one having ordinary skill in the art at the time the invention was made to

Art Unit: 2822

modify the semiconductor of Librizzi to include semiconductor mesa that comprises a silicon mesa as disclosed in Beyer because it aids in providing low leakage (For Example: See Column 2 Lines 20-24).

Additionally, since Librizzi and Beyer are both from the same field of endeavor, the purpose disclosed by Beyer would have been recognized in the pertinent art of Librizzi.

In regards to claims 4, 8, 12 and 16, Librizzi discloses the following:

a) the semiconductor substrate comprises a high resistivity semiconductor substrate (For Example: See Column 5 Lines 19-22).

7. Claims 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Librizzi et al. (U.S. Patent No. 6,429,502) in view of Clevenger et al. (U.S. Patent No. 6,573,565) and Hirabayashi (U.S. Patent No. 5,889,314).

In regards to claim 18, Librizzi fails to disclose the following:

a) the guard ring comprises a metal guard ring.

However, Hirabayashi discloses a semiconductor device that has a metal guard ring (For Example: See Column 5 Lines 1-14). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Librizzi to include a metal guard ring as disclosed in Hirabayashi because it aids in providing a low resistance (For Example: See Column 5 Lines 1-14).

Additionally, since Librizzi and Hirabayashi are both from the same field of endeavor, the purpose disclosed by Hirabayashi would have been recognized in the pertinent art of Librizzi.

In regards to claim 19, Librizzi fails to disclose the following:

a) the guard ring comprises a tungsten guard ring.

However, Hirabayashi discloses a semiconductor device that has a tungsten guard ring (For Example: See Column 5 Lines 1-14). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Librizzi to include a tungsten guard ring as disclosed in Hirabayashi because it aids in providing a low resistance (For Example: See Column 5 Lines 1-14).

Additionally, since Librizzi and Hirabayashi are both from the same field of endeavor, the purpose disclosed by Hirabayashi would have been recognized in the pertinent art of Librizzi.

8. Claims 1, 2, 5, 6, 9, 10, 13, 14 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Librizzi et al. (U.S. Patent No. 6,429,502) in view of Christensen et al. (U.S. Patent No. 6,645,796).

In regards to claim 1, Librizzi discloses the following:

- a) a semiconductor substrate (40) (For Example: See Figure 2);
- b) a buried insulation layer (42) over the semiconductor substrate (For Example: See Figure 2);
- c) a semiconductor mesa (28 or 34) over the buried insulation layer (For Example: See Figure 1 and Figure 2); and
- d) a guard ring (36 and 38) substantially surrounding the semiconductor mesa, and wherein the guard ring is arranged to provide RF isolation for the semiconductor mesa (For Example: See Figure 1 and Column 5 Lines 55-57).

In regards to claim 1, Librizzi fails to disclose the following:

- a) the guard ring extends through the buried insulation layer contacting the semiconductor substrate.

However, Christensen et al. ("Christensen") discloses a semiconductor device that has a guard ring (116) that extends through the buried insulation layer (910) contacting the semiconductor substrate (912) (For Example: See Figure 9). It would have been obvious to one

Art Unit: 2822

having ordinary skill in the art at the time the invention was made to modify the semiconductor of Librizzi to include a guard ring that extends through the buried insulation layer contacting the semiconductor substrate as disclosed in Christensen because it aids in providing a connection among the components (For Example: See Abstract).

Additionally, since Librizzi and Christensen are both from the same field of endeavor, the purpose disclosed by Christensen would have been recognized in the pertinent art of Librizzi.

In regards to claims 2, 6, 10 and 14, Librizzi discloses the following:

a) the semiconductor substrate comprises a high resistivity semiconductor substrate (For Example: See Column 5 Lines 19-22).

In regards to claims 5 and 13, Librizzi discloses the following:

a) the semiconductor substrate is doped in an area that is contacted by the guard ring (For Example: See Column 5 Lines 15 and 16).

In regards to claim 9, Librizzi discloses the following:

a) an insulating ring (26) between the guard ring and the semiconductor mesa, wherein the insulating ring surrounds the semiconductor mesa (For Example: See Figure 1).

In regards to claim 17, Librizzi discloses the following:

a) the guard ring comprises a low resistivity guard ring (For Example: See Column 6 Line 6).

9. Claims 3, 4, 7, 8, 11, 12, 15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Librizzi et al. (U.S. Patent No. 6,429,502) in view of Christensen et al. (U.S. Patent No. 6,645,796) and Beyer et al. (U.S. Patent No. 5,264,387).

In regards to claims 3, 7, 11 and 15, Librizzi discloses the following:

a) the semiconductor substrate comprises a silicon substrate, wherein the buried insulating layer comprises a buried silicon oxide layer (For Example: See Column 5 Lines 14-18).



Art Unit: 2822

In regards to claims 3, 7, 11 and 15, Librizzi fails to disclose the following:

- a) the semiconductor mesa comprises a silicon mesa.

However, Beyer et al. ("Beyer") discloses a semiconductor device that has semiconductor mesa that comprises a silicon mesa (For Example: See Column 3 Lines 15 and 16). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Librizzi to include semiconductor mesa that comprises a silicon mesa as disclosed in Beyer because it aids in providing low leakage (For Example: See Column 2 Lines 20-24).

Additionally, since Librizzi and Beyer are both from the same field of endeavor, the purpose disclosed by Beyer would have been recognized in the pertinent art of Librizzi.

In regards to claims 4, 8, 12 and 16, Librizzi discloses the following:

- a) the semiconductor substrate comprises a high resistivity semiconductor substrate (For Example: See Column 5 Lines 19-22).

10. Claims 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Librizzi et al. (U.S. Patent No. 6,429,502) in view of Christensen et al. (U.S. Patent No. 6,645,796) and Hirabayashi (U.S. Patent No. 5,889,314).

In regards to claim 18, Librizzi fails to disclose the following:

- a) the guard ring comprises a metal guard ring.

However, Hirabayashi discloses a semiconductor device that has a metal guard ring (For Example: See Column 5 Lines 1-14). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Librizzi to include a metal guard ring as disclosed in Hirabayashi because it aids in providing a low resistance (For Example: See Column 5 Lines 1-14).

Art Unit: 2822

Additionally, since Librizzi and Hirabayashi are both from the same field of endeavor, the purpose disclosed by Hirabayashi would have been recognized in the pertinent art of Librizzi.

In regards to claim 19, Librizzi fails to disclose the following:

a) the guard ring comprises a tungsten guard ring.

However, Hirabayashi discloses a semiconductor device that has a tungsten guard ring (For Example: See Column 5 Lines 1-14). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Librizzi to include a tungsten guard ring as disclosed in Hirabayashi because it aids in providing a low resistance (For Example: See Column 5 Lines 1-14).

Additionally, since Librizzi and Hirabayashi are both from the same field of endeavor, the purpose disclosed by Hirabayashi would have been recognized in the pertinent art of Librizzi.

### ***Conclusion***

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Monica Lewis whose telephone number is 571-272-1838. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on 571-272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300 for regular and after final communications.

ML

July 19, 2007



**MONICA LEWIS**  
**PRIMARY PATENT EXAMINER**